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Sughrue Mion Zinn Macpeak & Seas PLLC
2100 Pennsylvania Avenue NW
Washington, DC 20037-3213

EXAMINER	
PEREZ DAPLE, AARON C	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/693,976	CASAVANT ET AL.	
	Examiner	Art Unit	
	Aaron C Perez-Daple	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is in response to Amendment filed 5/6/04, which has been fully considered.

2. Claims 1-18 are presented for examination.

3. This Action is made FINAL.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claims 1-13** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, lines 8-10 of claim 1 recite limitations in which actions are initiated based on whether the witness graph is "empty" or "not empty." The specification, while enabling for a method of pruning a witness graph, does not disclose nor discuss a witness graph having "empty" and "not empty" states. In contrast, the specification discloses an iterative method for "pruning" or selecting certain paths in a witness graph to arrive at a final witness graph (see top of page 28). For the purpose of applying prior art, the Examiner interprets the limitations of lines 8-11 to mean performing simulation with an automatically generated testbench when

a conclusive result has not been previously reached. See also response to arguments, below.

6. As dependent claims, claims 2-13 suffer from the same deficiencies as claim 1.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claims 1-13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Lines 8-10 of claim 1 recite limitations in which actions are initiated based on whether the witness graph is "empty" or "not empty." Because the specification does not disclose nor discuss a witness graph having "empty" and "not empty" states (see rejection under 35 U.S.C. 112, first paragraph, above), it is not clear how to interpret these limitations.

Applicant has not recited any steps directed at pruning the witness graph, which would be necessary for limiting the paths to those demonstrating only property violation or property satisfaction as claimed. Because the "pruning" step is missing from claim 1 and is not explicitly recited until claim 5, it is difficult to interpret the claims. For the purpose of applying prior art, the Examiner finds that any teaching of testing paths in a witness graph (e.g. testing transitions in a state space) to reach a conclusive result with respect to a property is sufficient to meet the limitations found in lines 11-19 of claim 1. See also response to arguments below.

9. As dependent claims, claims 2-13 suffer from the same deficiencies as claim 1.

10. **Claim 14** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. Specifically, lines 33-34 recite the limitation "until one of said paths in said witness graph has been completely simulated." It is not clear what comprises "completely simulated." The Examiner interprets that "until...completely simulated" means until producing a conclusive result from the set consisting of property violation and property satisfaction.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. **Claims 1, 15 and 16** are rejected under 35 U.S.C. 102(b) as being anticipated by Geist et al. ("Coverage-directed test generation using symbolic techniques," In Proceedings of the International Conference on Formal Methods in CAD, pgs. 143-158, Nov. 1996.) (hereinafter Geist).

As for claim 1, Geist discloses a method of verification for a design comprising:

providing a description of said design (section 1, first paragraph, "The goal of hardware...to expected results.");

specifying correctness criteria for said design, wherein said correctness criteria are expressed as one or more correctness properties (section 1, first paragraph, "The goal of hardware...to expected results.");

abstracting said design description to provide an abstract model of said design (section 3, second paragraph, "Building the FSM Model...are not relevant.");

generating a witness graph for one of said one or more correctness properties based on a deterministic analysis of said abstract model (section 3, second paragraph, "Building the FSM Model…are not relevant.") ;

determining a conclusive result from the set consisting of property violation and property satisfaction, when said witness graph is empty (section 3.2, paragraphs two and three, "Model checking (21) is a…covers the transition."); and

generating a testbench automatically when said witness graph is not empty, and performing simulation with said testbench (section 3, paragraphs five to seven, "Generating Tests….the FSM model.");

wherein, when a property refers to universal path quantification, said witness graph includes paths demonstrating only said property violation, defining counter-examples (section 3.2, paragraphs two and three, "Model checking (21) is a…covers the transition.");

wherein, when said property refers to existential path quantification, said witness graph includes paths demonstrating only said property satisfaction, defining witnesses (section 3.2, paragraphs two and three, "Model checking (21) is a…covers the transition.");

wherein said conclusive result is said property satisfaction when said property refers to said universal path quantification (section 3.2, paragraphs two and three, "Model checking (21) is a…covers the transition."); and

wherein said conclusive result is said property violation when said property refers to said existential path quantification (section 3.2, paragraphs two and three, "Model checking (21) is a…covers the transition.").

13. As for claim 15, Geist discloses an automatic test bench generation method for hardware design, said hardware design being described in a hardware description and including correctness criteria expressed as a correctness property (section 1, first paragraph, "The goal of hardware…to expected results."), said automatic test bench generation method comprising:

generating a witness graph based on said hardware description (section 3, second paragraph, "Building the FSM Model…are not relevant.");

determining, based on said witness graph, embedded constraints for guiding vector generation (section 3, fourth paragraph, "Semantic Control path…PCI transaction types.");

generating a vector generator module including said embedded constraints (section 3, paragraphs five to seven, "Generating Tests….the FSM model."); and

generating, based on said correctness criteria, a monitor module for checking a correctness result with respect to said correctness property (section 3,2, paragraph 2, "Model checking…for test generation.").

14. As for claim 16, Geist discloses a method for assessing simulation coverage of a given set of simulation vectors for a given design, comprising:

providing a description of said design (section 1, first paragraph, "The goal of hardware…to expected results.");

specifying correctness criteria for said design, wherein said correctness criteria are expressed as one or more correctness properties (section 1, first paragraph, "The goal of hardware…to expected results.");

generating a witness graph for one or more of said correctness properties (section 3, second paragraph, "Building the FSM Model...are not relevant."); and

determining coverage of said witness graph, using said given set of simulation vectors,

by marking entities visited by said given set of simulation vectors in said witness graph, said entities being selected from the set consisting of states, transitions and paths ("marking" is inherent for determining if a transition has occurred; section 3.1, "In practice, one...to cover both cubes.").

15. **Claim 16** is rejected under 35 U.S.C. 102(b) as being anticipated by Gupta et al. ("Toward formalizing a validation methodology using simulation coverage," Design Automation Conference, 1997. Proceedings of the 34th , June 9-13, 1997 Pages:740 - 745.) (hereinafter Gupta). As for claim 16, Gupta discloses a method for assessing simulation coverage of a given set of simulation vectors for a given design, comprising:

providing a description of said design (Fig. 1, design specification);

specifying correctness criteria for said design, wherein said correctness criteria are expressed as one or more correctness properties (Fig. 1, design specification);

generating a witness graph for one or more of said correctness properties (Fig. 2); and

determining coverage of said witness graph, using said given set of simulation vectors,

by marking entities visited by said given set of simulation vectors in said witness graph, said entities being selected from the set consisting of states, transitions and paths (section 1, "An emerging paradigm...squashing and stalling).").

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. **Claim 1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta et al. ("Toward formalizing a validation methodology using simulation coverage," Design Automation Conference, 1997. Proceedings of the 34th , June 9-13, 1997 Pages:740 - 745.) (hereinafter Gupta) in view of Geist.

As for claim 1, Gupta discloses a method of verification for a design comprising:

providing a description of said design (Fig. 1, design specification);

specifying correctness criteria for said design, wherein said correctness criteria are expressed as one or more correctness properties (Fig. 1, design specification);

abstracting said design description to provide an abstract model of said design (section 4.1, "We consider the implementation...in the implementation.");

generating a witness graph for said one or more correctness properties based on a deterministic analysis of said abstract model (Fig. 2).

Gupta further teaches generating a test bench automatically and determining a conclusive result from the set consisting of property violation and property satisfaction (section 2, "A test model can...a comparison of outputs.").

Under the interpretation presented under the 35 U.S.C. 112 rejections above, although obvious to one of ordinary skill in the art and arguably inherent in Gupta, Gupta does not explicitly disclose reaching a conclusive result by finding either counter-examples or paths demonstrating property satisfaction. Geist teaches reaching a conclusive result by finding either counter-examples or paths demonstrating property satisfaction (section 3.2, paragraphs two and three, "Model checking (21) is a...covers the transition.").

It would have been obvious to one of ordinary skill in the art to modify Gupta based on the teachings of Geist by reaching a conclusive result by finding either counter-examples or paths demonstrating property satisfaction, because this would provide coverage of the abstract model while ensuring that each test obeys the constraints (section 3.2, first paragraph, "Given a temporal...obeys that assertion.").

18. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Geist in view of Hollander (US 6,182,258 B1) (hereinafter Hollander).

As for claim 2, Geist discloses the method for verification as set forth in claim 1, wherein said generation of said tesbench comprises:

determining embedded constraints for guiding vector generation based on said witness graph (section 3, fourth paragraph, "Semantic Control path...PCI transaction types.");

determining priorities for guiding said vector generation based on said witness graph (section 3, third paragraph, "Defining a Coverage Model…our verification methodology.");

generating a vector generator module including said embedded constraints and said priorites (section 3, paragraphs five to seven, "Generating Tests….the FSM model."); and

generating a monitor module, said monitor module checking said conclusive result (section 3, paragraphs five to seven, "Generating Tests….the FSM model.");

wherein, when said property refers to said universal path quantification, said vector generator module is generated so that said generated vectors are directed toward finding said counter-examples, and

wherein, when said property refers to said existential path quantification, said vector generator module is generated so that said generated vectors are directed toward finding said witnesses (section 3,2, paragraph 2, "Model checking…for test generation."); and

said simulation of said design, using said generated test bench, comprises checking said monitor module for property violation or satisifation (section 3,2, paragraph 2, "Model checking…for test generation.").

Geist does not specifically disclose generating the vectors using random patterns and applying said constraints as a filter to select desireable ones of said random patterns. Hollander teaches generating vectors using random patterns and applying constraints as a filter to select desireable ones of said random patterns (col. 2, lines 58-61, "Parameter-driven test…meeting known parameters.").

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Geist based on Hollander by generating the vectors using random patterns and applying said constraints as a filter to select desireable ones of said random patterns, because this would provide a method for generating suitable test vectors, as taught by Hollander (col. 2, lines 58-61, "Parameter-driven test...meeting known parameters.").

19. As for claim 3, Geist teaches a method of verication similar to that of claim 2, wherein:

said embedded constraints are derived from transition conditions in said witness graph (section 3, fourth paragraph, "Semantic Control path...PCI transaction types."); and

said priorities are associated with transitions in said witness graph (section 3, third paragraph, "Defining a Coverage Model...our verification methodology.").

20. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Geist in view of Hollander and in further view of applicant's admitted prior art (pg. 24, lines 19-21).

Neither Geist nor Hollander specifically disclose generating priorities based on the methods recited in lines 3-5 of claim 4. However, applicant admits that these methods are known, as taught by the cited references <15, 17, 24 and 29>. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Geist and Hollander by generating priorities based on one or more of distance to targets, transition probabilities and simulator trace data, because

these are known methods for prioritizing state space searching, as taught by Applicant.

Allowable Subject Matter

21. **Claim 17** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Specification

22. Objections to the title are hereby withdrawn in view of Amendment.

Drawings

23. Objections to Fig. 1 are hereby withdrawn in view of Amendment.

24. Objections to Fig. 17 are hereby withdrawn in view of Remarks, which are found persuasive.

Claim Objections

25. Objections to claim 2 are hereby withdrawn in view of Remarks, which are found persuasive.

26. Objections to claim 4 are hereby withdrawn in view of Remarks, which are found persuasive.

Claim Rejections under 35 U.S.C. 112, first paragraph

27. With respect to the 35 U.S.C. 112, first paragraph, rejection of claims 1-13, Applicant's arguments found on pg. 20 of the Remarks have been fully considered but they are not persuasive. Applicant cites pgs. 17-18 and 27 of the specification in support of the use of the terms "empty" and "not empty" with reference to the witness graph. First, the Examiner finds that *none* of the cited passages discuss an empty or not empty witness graph. Applicant appears to take the position that an empty or not empty witness graph is implied by the cited passages. However, the Examiner respectfully disagrees.

Applicant draws on subject matter found in the first full paragraph of pg. 17, asserting, "...if the property is determined as true or false, the witness graph is empty, e.g. if the initial state does not belong to the set upper, the property is false. If the property is false or true, then no existing paths are present. If it is determined that *no existing paths are present* or that *initial state does not belong to the set,* then clearly no paths for the witness graph can be generated, and as a result, the witness graph will be empty...." The cited passages simply do not provide support for Applicant's assertions. As detailed on pg. 17, if the initial state does not belong to one of the sets *upper* or *negative*, depending on whether the property is universal or existential, then a conclusive result is reached. However, the fact that an *initial state* is not part of a set of states, is not equivalent to the witness graph being empty. From the disclosure, it appears that either the initial model checking is performed *prior* to the generation of a witness graph, or that the witness graph is itself composed of the states found in the sets *upper* or *negative*. In the first case, the witness graph would not be generated at

all, since a conclusive result would already have been reached. In the second case, the witness graph would not be empty but would contain the states for the sets upper or negative. Support for this interpretation is found in the first two paragraphs of pg. 15, which recite that model checking is used to *precompute* a set of states which are likely to be witnesses (or counter-examples) of the property.

Moreover, for the case when a witness graph is generated (i.e. "not empty"), the conclusive result appears to derive from the ability (or inability) to identify a path(s) demonstrating either property satisfaction or property violation from the witness graph. In this case, the witness graph would also not be empty, since the paths it contains are relied upon to reach the conclusive result. Support for this interpretation is found throughout the specification, especially pgs. 8-9, 15 and the second full paragraph of pg. 27.

Therefore, the rejection of claims 1-13 under 35 U.S.C. 112, first paragraph, is properly maintained.

Claim Rejections under 35 U.S.C. 112, second paragraph

28. With respect to the 35 U.S.C. 112, second paragraph, rejection of claims 1-13, Applicant's arguments found on pgs. 21-24 of the Remarks have been fully considered but they are not persuasive.

For the reasons cited above in support of the rejection of claims 1-13 under 35 U.S.C. 112, first paragraph, the use of the terms "empty" and "not empty" with respect to the witness graph is found indefinite. The disclosure does not provide proper support for these limitations in the claim, and the Examiner is unable to

interpret the claims in a manner which is consistent with the disclosure or even self-consistent within the claims. The Examiner also notes that the use of the term "said conclusive result" in lines 16 and 18 appears to have improper antecedent basis, because it would not be the same conclusive result as the one determined previously (e.g. when the witness graph is claimed as "empty").

The Examiner notes Applicant's amendment of claim 1 to recite "one of said one or more correctness properties." This amendment helps to clarify the claims but is not sufficient to overcome the rejection. Although the disclosure does state on pg. 9 that the witness graph is used for enumerating witnesses or counter-examples of the property, it is also clear that all of the states in the witness graph do not necessarily demonstrate *only* property violation or property satisfaction. Rather, the pruning process disclosed on pgs. 19-20 is directed to limiting the witness graph in this manner. Prior to pruning, the witness graph only identifies states that are *likely* to exhibit the property violation or property satisfaction. Furthermore, for the case with a ("not empty") witness graph, a conclusive result could not be reached without pruning. Therefore, it is clear that claim 1 is missing the necessary step of pruning.

For all of these reasons, the rejection of claims 1-13 under 35 U.S.C. 112, second paragraph, is properly maintained.

29. The rejection of claims 2 and 15 under 35 U.S.C. 112, second paragraph, is hereby withdrawn in view of Remarks, which are found persuasive.

30. With respect to the 35 U.S.C. 112, second paragraph, rejection of claim 14, Applicant's arguments found on pg. 24 of the Remarks have been fully considered but they are not persuasive. Specifically, the claims do not recite determining that a

conclusive result was reached nor that the path has been fully expanded. The term "completely simulated" by itself is not sufficient such that one of ordinary skill in the art would be able to determine the scope of the claims.

31. The rejection of claim 18 under 35 U.S.C. 112, second paragraph, is hereby withdrawn in view of Amendment.

102 Claim Rejections

32. With respect to the 35 U.S.C. 102(b) rejection of claims 1, 15 and 16 as anticipated by Geist, Applicant's arguments found on pgs. 25-28 of the Remarks have been fully considered but they are not persuasive. On pages 25-26, Applicant makes several general assertions which are not directed towards any specific limitations of the claims. Therefore, these assertions are moot. With respect to the claim limitations, Applicant asserts that Geist fails to teach or suggest *generating a witness graph*. The Examiner respectfully disagrees. As recited on pg. 9, first full paragraph, of the specification, a witness graph "is used to denote the collection of states and transitions which are useful for enumerating witnesses or counter-examples for the required property." The Examiner finds that the FSM (finite-state model) of Geist is precisely such a witness graph, as explicitly detailed in sections 3-3.2. The Examiner notes that no specific format of the witness graph has been claimed.

Next, the Examiner respectfully disagrees with Applicant's assertion that Geist fails to teach *generating a testbench automatically*. In section 3, Generating Tests, Geist discloses systems for performing exactly this function (e.g. translator and concretizer).

Finally, Applicant asserts that Geist fails to teach or suggest *defining witnesses when the property refers to existential path qualification.* The Examiner respectfully disagrees. The coverage model set of Geist (defined in section 3.1) comprises witnesses for the property when the property refers to existential path quantification.

For all these reasons, claims 1, 15 and 16 are properly rejected under 35 U.S.C. 102(b) as anticipated by Geist.

33. With respect to the 35 U.S.C. 102(b) rejection of claim 16 as anticipated by Gupta, Applicant's arguments found on pg. 28 of the Remarks have been fully considered but they are not persuasive. Applicant asserts that Gupta fails to teach or suggest *generating a witness graph for one or more correctness properties.* As recited on pg. 9, first full paragraph, of the specification, a witness graph "is used to denote the collection of states and transitions which are useful for enumerating witnesses or counter-examples for the required property." The broadest reasonable interpretation of the term "witness graph" is therefore a collection of states and transitions. Merely being useful for enumerating witnesses or counter-examples is not sufficient to *require* them. Moreover, since the transition tours are used to identify errors, as described in section 4.3, they are in fact used to find *witnesses* of these errors (i.e. the transition which demonstrates the error is a *witness* to the error). Whether or not the transition tour includes all of the states and transitions of a test space, or merely a subset of them, has no bearing on the claim.

Therefore, claim 16 is properly rejected under 35 U.S.C. 102(b) as anticipated by Gupta.

103 Claim Rejections

34. With respect to the rejection of claim 1 under 35 USC 103(a) as unpatentable over Gupta in view of Geist, Applicant's arguments on pg. 29 of the remarks have been fully considered but are not persuasive. For the reasons given above in defense of the 102 Claim Rejections, Geist and Gupta properly anticipate the limitations of claim 1. Furthermore, the fact that Gupta includes Geist as a reference is not sufficient to show that it would not have been obvious to combine the teachings. The test is rather what their combined teachings would suggest to one of ordinary skill in the art. Moreover, the statement in Gupta that "most of these coverage metrics do not provide a measure of the design error coverage" has no direct bearing on the claims, nor does it preclude that other features of the invention would be logical to combine. Finally, one of ordinary skill in the art might be motivated to combine the references precisely in order to provide a measure of the design error coverage.

35. With respect to the rejection of claims 2 and 3 under 35 USC 103(a) as unpatentable over Geist in view of Hollander, Applicant's arguments on pgs. 29-30 of the remarks have been fully considered but are not persuasive. Since Geist has been shown to properly anticipate all the limitations of claim 1, Hollander does not have to teach these features. Therefore, claims 2 and 3 are properly rejected for the same reasons.

36. With respect to the rejection of claim 4 under 35 USC 103(a) as unpatentable over Geist in view of Hollander and in further view of AAPA, Applicant's arguments on pgs. 29-30 of the remarks have been fully considered but are not persuasive. Since Geist has been shown to properly anticipate all the limitations of claim 1, Hollander

and AAPA do not have to teach these features. Therefore, claim 4 is properly rejected for the same reasons.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron C Perez-Daple whose telephone number is (703) 305-4897. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (703) 305-8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8/12/04

Aaron Perez-Daple

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100